

VME Intensity Monitor - Support #13359

Update Pxie Gate Width Calibration Mode

07/27/2016 04:25 PM - Roger Tokarek

Status:	Work in progress	Start date:	07/27/2016
Priority:	Normal	Due date:	
Assignee:	Roger Tokarek	% Done:	80%
Category:	ACNET	Estimated time:	6.00 hours
Target version:		Spent time:	0.00 hour
Description			
The <i>gate width calibration</i> mode requested by Engineering is updated to reflect the change of gate width from a 2B to a 4B register. Acnet devices for each ADC board are created.			

History

#1 - 07/27/2016 05:25 PM - Roger Tokarek

Calibration Mode

To **enter calibration mode**, in a pxint telnet session for example, the user types: gwcenable adcMapping, "microseconds"

```
gwcenable 0, "64.5"
```

Microseconds is a decimal value and must be in quotes. The first parameter, adcMapping, indicates which ADCs are set to calibration mode. See the Acnet Devices Table below. **Bug, adcMapping does not match ADC #1.**

To **disable calibration mode** - that is to return to normal operation:

```
gwcdisable 0
```

The user needs to remember to disable the calibration mode for the particular ADC they were working with.

Help is available:

```
helpgw
```

Acnet Devices

See D150, pxie pages 2-9 for gate widths by ADC and page 10 for a one page list of all gate widths. (July 27, 2016)

ADC	Address	Acnet	adcMapping
0	0x0000	P:L20TOW	0
1	0x1000	P:M01EPW	???
2	0x2000	P:M01PTW	2
3	0x3000	P:MX2PTW	3
4	0x4000	P:MX1FPW	4

#2 - 07/29/2016 09:08 AM - Roger Tokarek

- Status changed from Resolved to Work in progress

- % Done changed from 100 to 80